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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,182	02/06/2001	Michael Scurry	A-69575/SFC/WEN	9026

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EXAMINER

THANGAVELU, KANDASAMY

ART UNIT PAPER NUMBER

2123

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

14

Office Action Summary	Application No.	Applicant(s)	
	09/778,182	SCURRY, MICHAEL	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 February 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>March 22, 2001 and</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-22 of the application have been examined.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on March 22, 2001 and August 21, 2002 together with copies of the patents and papers. The patents and papers have been considered in reviewing the claims.

Drawings

3. The drawings are objected to; see a copy of Form PTO-948 for an explanation.

Specification

4. The disclosure is objected to because of the following informalities:

Page 4, Lines 17-18, "that are unnecessary for testing custom and semi-custom ICs, which usually relative low gate count" appears to be incorrect and it appears that it should be "that are unnecessary for testing custom and semi-custom ICs, which have usually relative low gate count".

Appropriate correction is required.

Claim Objections

5. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

6. Claim 3 is objected to because of the following informalities:

Claim 3, Line 1, "The ISD according to claim 1, wherein is using a Universal Test & Operations Physical Interface to ATM (UTOPIA) interface" appears to be incorrect and it appears that it should be "The ISD according to claim 1, wherein interface software is using a Universal Test & Operations Physical Interface to ATM (UTOPIA) interface".

Appropriate correction is required.

Claim Interpretations

7. In Claim 3, Line 1, "The ISD according to claim 1, wherein is using a Universal Test & Operations Physical Interface to ATM (UTOPIA) interface" is interpreted as "The ISD according to claim 1, wherein the interface software is using a Universal Test & Operations Physical Interface to ATM (UTOPIA) interface".

Claim Rejections - 35 USC § 102

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8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

9. Claims 1, 2, 6, 7, 9, 10, 14, 16, 17 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by **Lin et al.** (U.S. Patent 6,389,379).

9.1 **Lin et al.** teaches coverification system and method. Specifically, as per claim 1, **Lin et al.** teaches an In-system-Developer (ISD) for developing a customized integrated circuit (IC) for use in an external system while connected to the external system (Fig 1; Fig 3; Abstract, L6-8; CL3, L52-61); the ISD comprising:

a development board for holding an IC core, the development board having a one or more ports for transmitting data and signals to and from the IC core (Fig 1; Fig 3; Abstract, L16-18; Abstract, L19-21; CL24, L4-27; Fig 22);

a data processing system coupled to the development board (Fig 1; Fig 3);

hardware descriptor language (HDL) software capable of being executed by the data processing system to configure the IC core to form the IC (Fig. 26-29; CL28, L15-19);

at least one input-output (IO) cable coupling the ports to the external system for transmitting data from the external system to the IC core and transmitting signals from the IC core to the external system (Fig. 10; CL46, L46-57); and

interface software having program code adapted to translate Register Transfer Level (RTL) code to code used by the HDL software, thereby enabling the design to be tested as it is being developed (CL28, L15-19; CL28, L58 to CL29, L13; CL54, L18-31; CL45, L31-37).

Per claim 2: **Lin et al.** teaches that the interface software further comprises program code adapted to assign predetermined signal in the RTL code to predetermined ports on the development board (Fig 21 and 22(1); CL66, L29-59; CL77, L46-56; CL80, L1-40).

Per claim 6: **Lin et al.** teaches that the interface software comprises program code adapted to enable designating ports on the development board to be monitored (Fig 21 and 22(1); CL66, L29-59; CL77, L46-56; CL80, L1-40).

Per claim 7: **Lin et al.** teaches that the interface software comprises program code adapted to enable designating an output to be recorded in a VCD file (CL47, L55-63).

9.2 As per Claims 9, 10 and 14, these are rejected based on the same reasoning as Claims 1, 2 and 7 supra. Claims 9, 10 and 14 are method claims reciting the same limitations as Claims 1, 2 and 7, as taught throughout by **Lin et al.**

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9.3 As per Claims 16, 17, 21 and 22, these are rejected based on the same reasoning as Claims 1, 2, 6 and 7 supra. Claims 16, 17, 21 and 22 are computer program product claims reciting the same limitations as Claims 1, 2, 6 and 7, as taught throughout by **Lin et al.**

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 3, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin et al.** (U.S. Patent 6,389,379) in view of **Kejriwal et al.** (U.S. Patent 6,704,794).

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11.1 As per claim 3, **Lin et al.** teaches the ISD of claim 1. **Lin et al.** does not expressly teach that the interface software is using a Universal Test & Operations Physical Interface for ATM (UTOPIA) interface and wherein the interface software is adapted to translate UTOPIA RTL code. **Kejriwal et al.** teaches that the interface software is using a Universal Test & Operations Physical Interface for ATM (UTOPIA) interface and wherein the interface software is adapted to translate UTOPIA RTL code (CL3, L25-43; CL21, L62 to CL22, L9), because cells are data used to transport data packets through a network and various interfaces in packet passage through the ports may be implemented using UTOPIA based interface (CL3, L37-44). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the ISD of **Lin et al.** with the ISD of **Kejriwal et al.** that included the interface software using a Universal Test & Operations Physical Interface for ATM (UTOPIA) interface and wherein the interface software was adapted to translate UTOPIA RTL code. One would be motivated because cells were data used to transport data packets through a network and various interfaces in packet passage through the ports might be implemented using UTOPIA based interface.

11.2 As per Claims 11 and 18, these are rejected based on the same reasoning as Claim 3, supra. Claims 11 and 18 are method and computer program product claims reciting the same limitations as Claim 3, as taught throughout by **Lin et al.** and **Kejriwal et al.**

12. Claims 4, 5, 12, 13, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin et al.** (U.S. Patent 6,389,379) in view of **Stapleton et al.** (U.S. Patent 6,106,565).

12.1 As per claims 4 and 5, **Lin et al.** teaches the ISD of claim 1. **Lin et al.** does not expressly teach that the interface software comprises program code adapted to enable assigning a clock speed for the IC core; and program code adapted to determine if the IC core is capable of operating at the assigned clock speed. **Stapleton et al.** teaches that the interface software comprises program code adapted to enable assigning a clock speed for the IC core; and program code adapted to determine if the IC core is capable of operating at the assigned clock speed (CL2, L38-41; CL5, L65 to CL6, L9), because the emulated processor operates at different clock speed from the emulating processor and the development system (ISD) includes a clock circuit for generating requisite clock frequencies (CL2, L38-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the ISD of **Lin et al.** with the ISD of **Stapleton et al.** that included the interface software comprising program code adapted to enable assigning a clock speed for the IC core; and program code adapted to determine if the IC core was capable of operating at the assigned clock speed. One would be motivated because the emulated processor would operate at different clock speed from the emulating processor and the development system (ISD) would include a clock circuit for generating requisite clock frequencies.

12.2 As per Claims 12, 13, 19 and 20, these are rejected based on the same reasoning as Claims 4 and 5, supra. Claims 12, 13, 19 and 20 are method and computer program product claims reciting the same limitations as Claim 3, as taught throughout by **Lin et al.** and **Stapleton et al.**

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin et al.** (U.S. Patent 6,389,379) in view of **Butts et al.** (U.S. Patent 6,002,861).

13.1 As per claim 8, **Lin et al.** teaches the ISD of claim 1. **Lin et al.** teaches that IC core is selected from a group consisting of Field Programmable Gate Arrays (Fig. 10, Item 325; CL24, L28-31; CL45, L63-64; CL70, L46-50). **Lin et al.** does not expressly teach that IC core is selected from a group consisting of Electronically Reconfigurable Gate Arrays. **Butts et al.** teaches that IC core is selected from a group consisting of Electronically Reconfigurable Gate Arrays (Abstract, L1-10; CL1, L21-24), because the reconfigurable interconnect permits the digital network realized on the interconnect chips to be changed at will suited for simulation and emulation (Abstract, L5-10), to permit fast and detailed analysis of a logic circuit's operation (CL1, L29-30). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the ISD of **Lin et al.** with the ISD of **Butts et al.** that included IC core selected from a group consisting of Electronically Reconfigurable Gate Arrays. One would be motivated because the reconfigurable interconnect would permit the digital network realized on the interconnect chips to be changed at will suited for simulation and emulation to permit fast and detailed analysis of a logic circuit's operation.

14. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin et al.** (U.S. Patent 6,389,379) in view of **Takahashi et al.** (U.S. Patent 6,061,283), and further in view of **Buckley, JR** (U.S. Patent Application 2002/0078424).

14.1 As per claim 15, **Lin et al.** teaches the method of claim 9. **Lin et al.** teaches that test bench components control simulation/emulation by reading test vectors, checking changes in value, performing value change dump, checking constraints on signal values and writing out test vectors (CL29, L57-66).

Lin et al. does not expressly teach the step of generating a test bench using data in the VCD file to enable self-checking of the IC core. **Takahashi et al.** teaches creating test pattern data from the value change dump file (CL2, L54-65), so the test patterns can be debugged using the test simulator prior to use in test of the LSI device (CL2, L66 to CL3, L8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Lin et al.** with the method of **Takahashi et al.** that included creating test pattern data from the value change dump file. One would be motivated because that would allow the test patterns to be debugged using the test simulator prior to use in test of the LSI device.

Buckley, JR teaches creating a design verification test bench using the test patterns generated by the Automatic test pattern generator (ATPG) and pre-existing test bench HDL design templates suitable for the identified circuit classes (Page 1, Para 0001 and Para 0005), because that allows creation of complex tests automatically, rapidly and in volume and relatively free of error, enabling bringing a large design up to speed as rapidly as possible (Page 1, Para 0004 and Para 0008). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Lin et al.** with the method of **Buckley, JR** that included creating a design verification test bench using the test patterns generated. One would be motivated because that would allow creation of complex tests automatically, rapidly and in

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volume and relatively free of error, enabling bringing a large design up to speed as rapidly as possible.

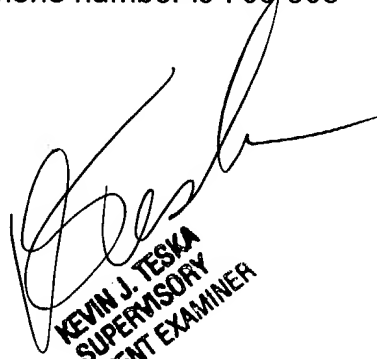
Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
May 6, 2004



KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER